

WHAT IS CLAIMED IS:

1. A method of regulating a target system, comprising the steps of:
providing a reference signal;
generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;
5 providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;
comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;
10 generating a control signal dependent upon said comparison; and
providing said control signal as an input to said target system.

2. The method of regulating a target system of claim 1, wherein said comparing step comprises substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train.

3. The method of regulating a target system of claim 2, wherein said step of generating said control signal comprises the substep of generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train
5 and said feedback pulse train.

*Sub
a1* 4. The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substeps of:
counting up from zero with a first proportional clock CP1 at a frequency fP1 when
said digital signals of said proportional error pulse train are in a high state;

5 ~~resetting said first proportional clock CP1 to zero when said digital signals of said~~
proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second
proportional clock CP2 each time said first proportional clock CP1 transitions from a high
state to a low state;

10 counting down from said loaded current value with said second proportional clock
CP2 at a frequency fP2 until a zero value is reached; and

determining a proportional error term representing a time average of a signal
which is held high while said second proportional clock CP2 is in a high state and held
low while said second proportional clock CP2 is in a zero state, said control signal being
15 ~~dependent upon said proportional error term.~~

5 5. The method of regulating a target system of claim 3, wherein said step of
generating said control signal comprises the further substep of generating an error
direction pulse train including a plurality of digital signals, each said digital signal
representing a directionality of said error between said corresponding pair of aligned
digital signals.

Sub
CP2 6. ~~The method of regulating a target system of claim 5, wherein said step of~~
generating said control signal comprises the further substeps of:

5 counting up from zero with a first integral clock CI1 at a frequency fI1 when said
digital signals of said proportional error pulse train are in a high state and said digital
signals of said error direction pulse train are simultaneously in a high state;

counting down with said first integral clock CI1 at said frequency fI1 when said
digital signals of said proportional error pulse train are in a high state and said digital
signals of said error direction pulse train are in a low state;

~~determining a derivative error term representing a time average of a signal which is held high while said second derivative clock CD2 is in a high state and held low while said second derivative clock CD2 is in a zero state, said control signal being dependent upon said derivative error term.~~

8. The method of regulating a target system of claim 1, wherein said frequency of said feedback pulse train varies with time.

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